3-8. QAV

Analog Input Point
(Syle 7379A21G01 through G09)

3-8.1. Description

Groups 01through G09 are applicable for use in the CE MARK Certified System

The QAV card converts an analog field signal to digital data (see Figure 3-54). (For new applications, a QAX card is recommended). The digital data is the summation of a frequency that has been counted for a time period. The time period is a multiple of the power line frequency (50 or 60 Hz).

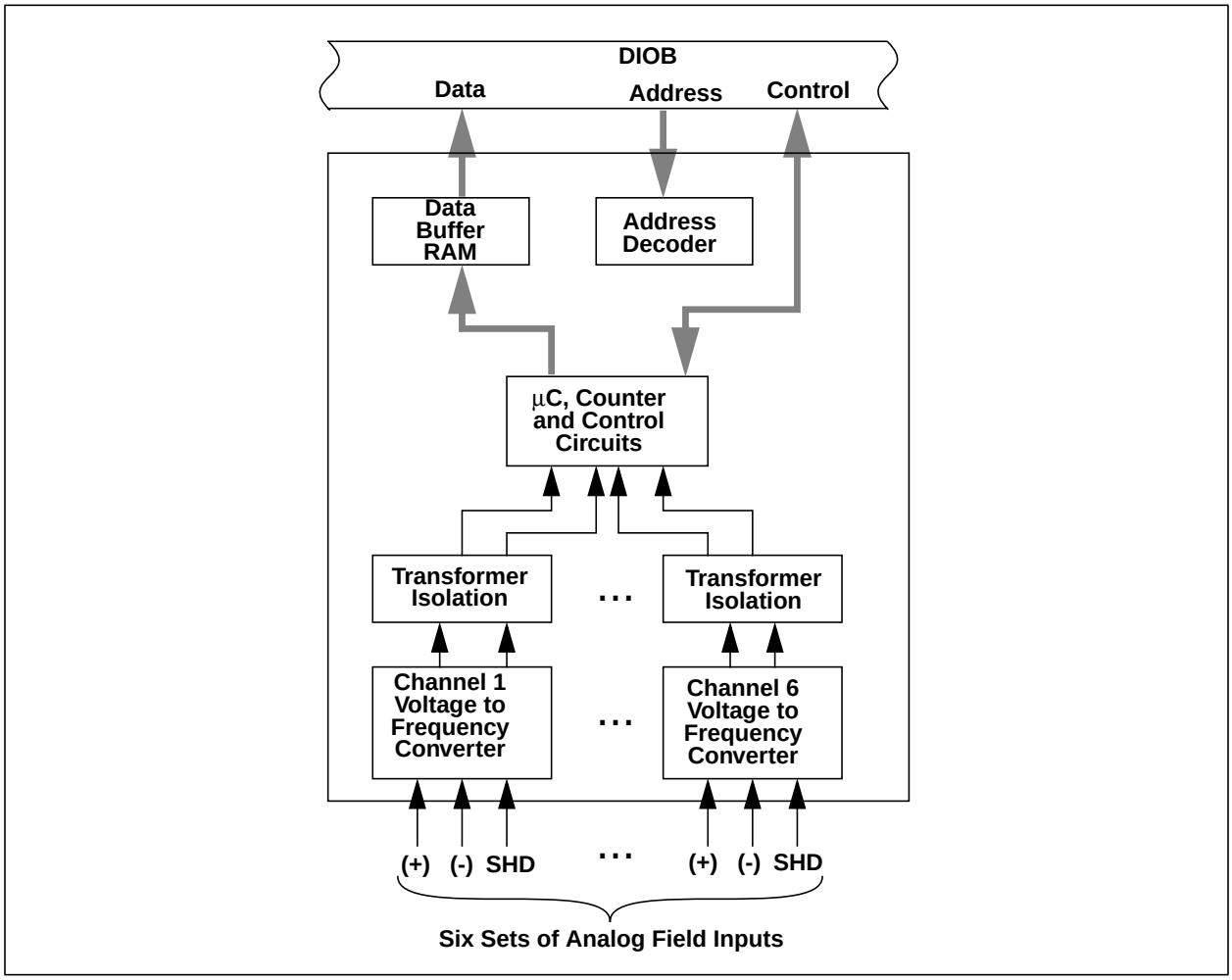

Figure 3-54. QAV Block Diagram

Each QAV card contains six individually isolated voltage-to-frequency converter circuits (channels). The output of each input circuit is processed by a common microcomputer and the resulting digital data is multiplexed to the Distributed Input/Output Bus (DIOB) as a 13-bit word.

Figure 3-55 shows a typical control system configuration using QAV cards. The QTB card is necessary for applications where large variations of power line frequency exist to obtain a high normal mode rejection. Up to 30 QAV cards (180 channels) can be used with one DIOB controller.

Cards equipped with the thermocouple temperature compensation feature use channel 6 for the on-card temperature sensor. The channel is read every time the card performs an auto-calibration cycle. The on-card temperature sensor eliminates the need for external sensor boards, and ensures field temperature accuracy.

The QAV card uses an electrical isolation circuit (transformer) to separate the analog input from the digital counting circuits. The isolation circuit provides power for each analog input channel in addition to precise timing from a stable frequency which is generated on the digital side of the QAV card circuits.

Each analog input circuit contains circuitry for signal conditioning, biasing, auto-zero and gain correction, open thermocouple detection (not available on G04 and G05 QAV cards) and a clocked voltage-to-frequency converter.

Offset and gain correction factors are calculated on a periodic basis by the QAV card microcomputer. The frequency of the offset and gain calibration cycle is determined by a constant which has been programmed into the memory of the system controller.

Two known potentials on the analog section of the QAV card are used as standards for offset and gain calibrations. One standard is a 0 VDC (shorted input), which is used to determine the offset correction factor. The second calibrating potential (gain) is derived from a separate, stable voltage reference which is set approximately −150% of the maximum expected analog input value. The gain correction factor is compared to a 16-bit calibration constant which is programmed into the memory of the system controller at the time of factory card calibration. The calibration constant is necessary because the QAV card has no mechanical adjusting devices (such as potentiometers, and so on). This method yields a trimmer (or pot) -less calibrating method.

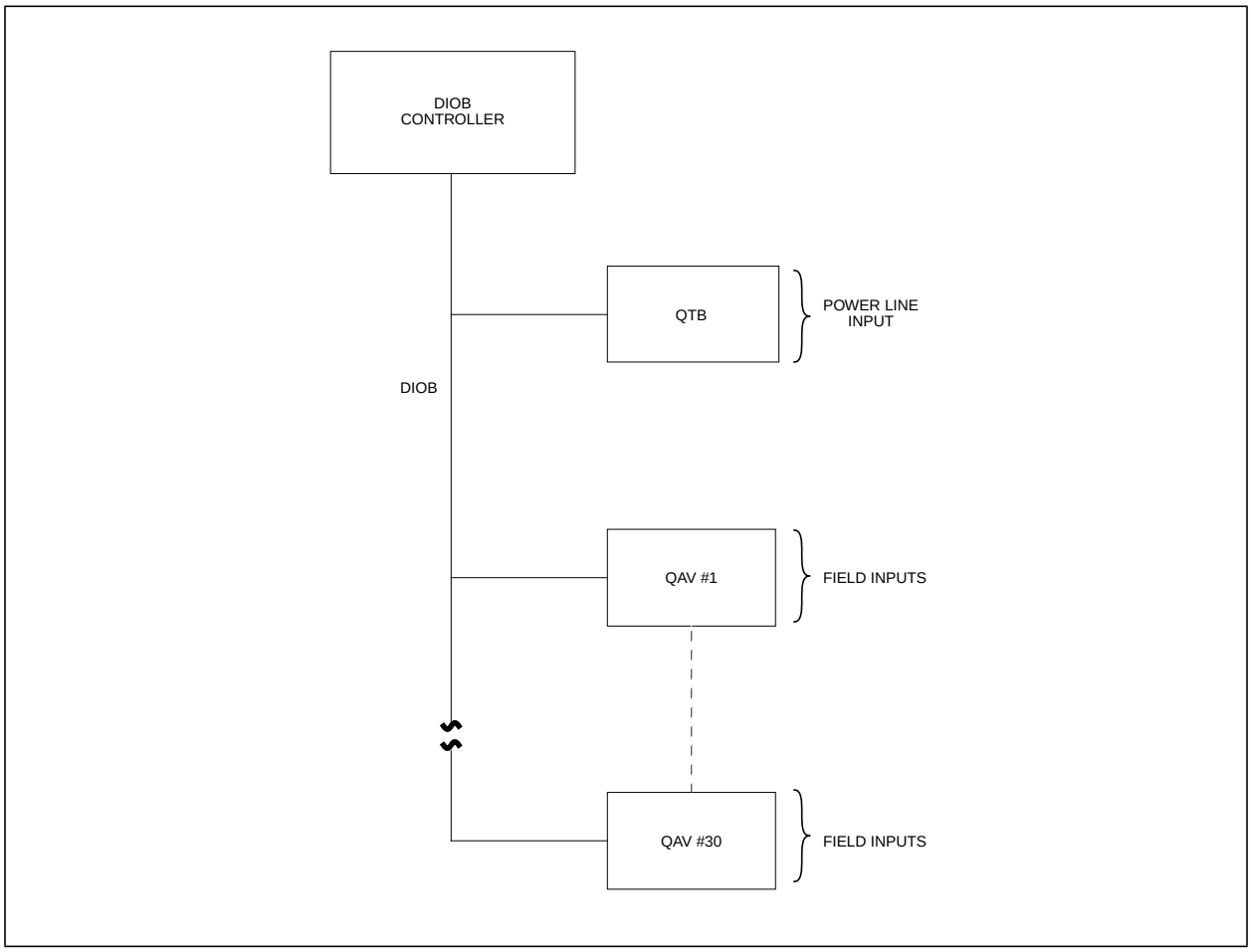

Figure 3-55. QAV Typical Control System Using QAV Cards

The QAV card microcomputer is programmed to “limit check” (reasonability check) the offset correction factor for each analog input channel. Failure of the reasonability check causes bit 14 (offset over-range) of the output data for that channel to be set to a logical zero. A failure on two or more channels causes bit 15 (IMOK bit) of the output data to be set to a logical zero which indicates card trouble to the system controller.

Note

The two-channel failure feature is available on QAV cards at levels 1QAV through 4QAV.

Bit 15 is also set to zero during the power-up routine of the QAV card. The QAV microcomputer is reset at this time and conversion of data is begun when the reset control is removed and the QAV card buffer memory is updated. Bit 15 is reset to a logical 1 after a warm-up pause is completed. The length of the warm-up pause is determined by a programmed constant in the memory of the system controller.

- G01 and G07 [1]: –5 to +20 mVDC (–20 to +20 mVDC at reduced accuracy [2]); 500 Ω maximum source impedance.
- G02 and G08[1]: –12.5 to +50 mVDC (–50 to +50 mVDC at reduced accuracy[2]); 500 Ω maximum source impedance.
- G03 and G09[1]: –25 to +100 mVDC (–100 to +100 mVDC at reduced accuracy[2]); 1 KΩ maximum source impedance.
- G04: –12.5 to +50 mVDC (–50 to +50 mVDC at reduced accuracy[2]); 500 Ω maximum source impedance (G04 is not available with the Open Thermocouple Detection feature).
- G05: –25 to +100 mVDC (–100 to +100 mVDC at reduced accuracy[2]); 1 KΩ maximum source impedance (G05 is not available with the Open Thermocouple Detection feature).
- G06: –12.5 to +50 mVDC (–50 to +50 mVDC at reduced accuracy[2]); 1 KΩ maximum source impedance.

[1]Level 8 QAV and later artwork support groups 1-3 **without** "On-Card" thermocouple compensation. Groups 7-9 are identical to Level 6 QAV groups 1-3 **with** "On-Card" thermocouple compensation. If "On-Card" thermocouple compensation is required, order groups 7-9 in place of groups 1-3 respectively.

[2]Reduced reference accuracy is ±0.20 percent of the upper range value (±10 µV, ±1/2 LSB at 99.7 percent confidence.

3-8.2. Features

Each QAV card has the following features:

- IEEE surge withstand capability
- Auto zero, auto gain correction
- Electrical isolation on all channels
- On-card digital memory (buffer)
- Open thermocouple detection (This feature is not available on G04 and G05 QAV cards.)
- Common mode rejection
- Normal mode rejection
- Automatic reasonability test (shorted input)
- Auto-conversion check
- Jumper selectable 50/60 Hz operation
- On-card thermocouple temperature compensation (Available on QAV cards at level 6 QAV)

The QAV card is designed to be mounted in a standard Q-line card cage. Connection to the control system is made by a 34-pin rear-edge backplane connector which interfaces the UIOB or DIOB and a 56-pin front-edge connector, which connects to field terminals.

Block Diagram

A block diagram of one of the six analog sections of the QAV card is shown in Figure 3-56. Figure 3-57 shows a block diagram of the QAV digital circuits. Figure 3-58 shows a flow diagram of the QAV card analog-to-digital conversion process.

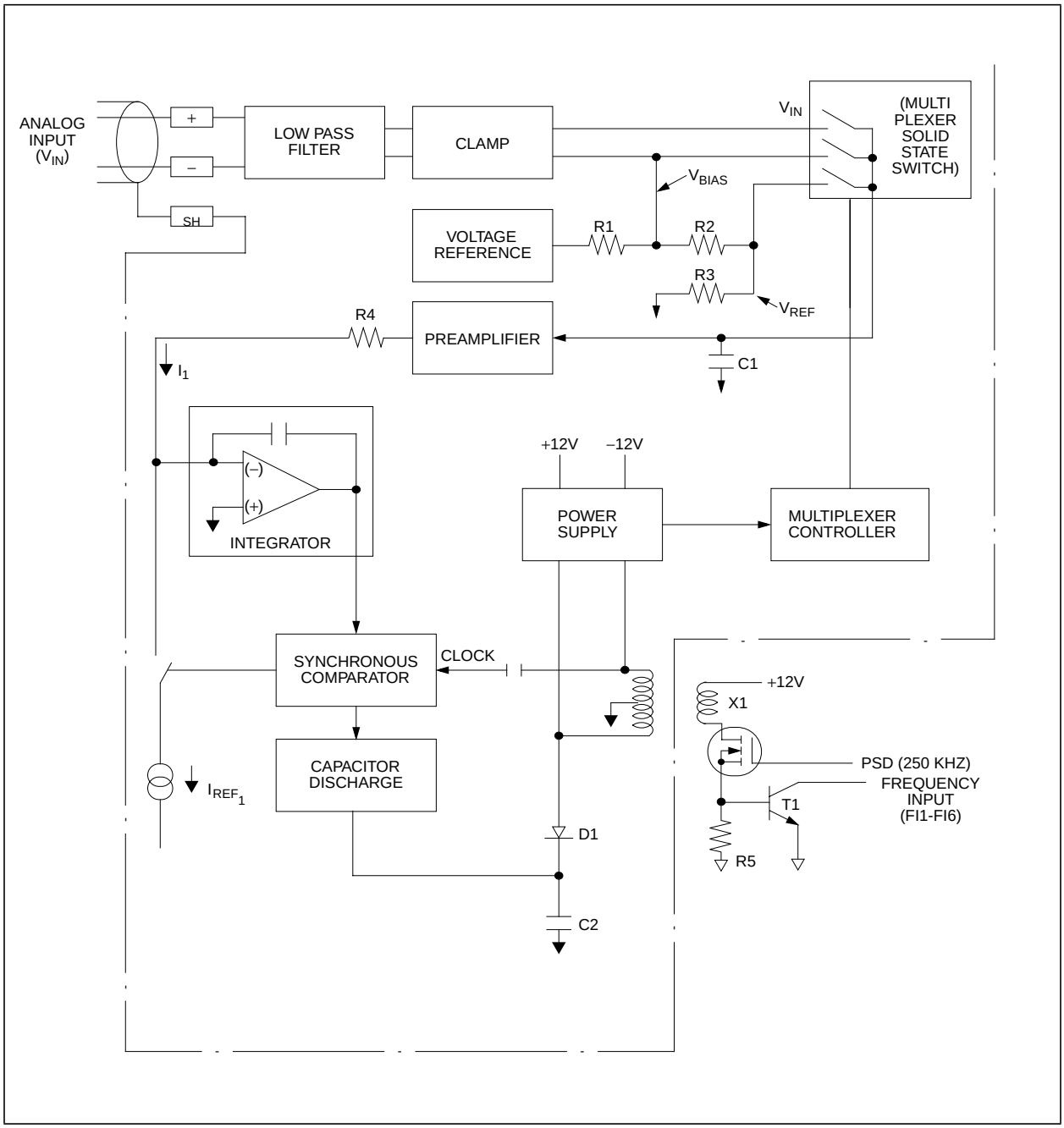

Figure 3-56. QAV Analog Input Circuits Block Diagram

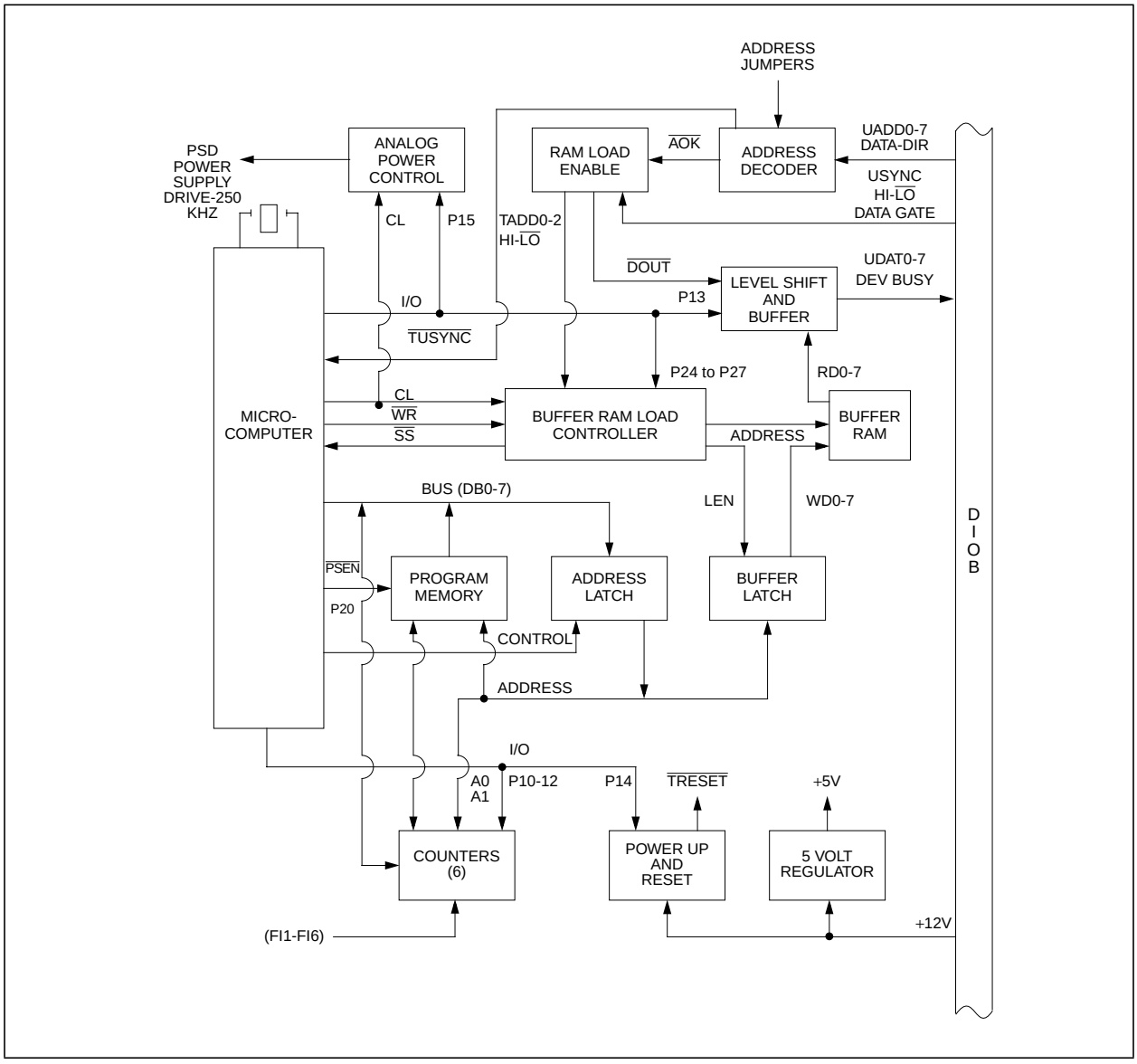

Figure 3-57. QAV Card Digital Circuits Block Diagram

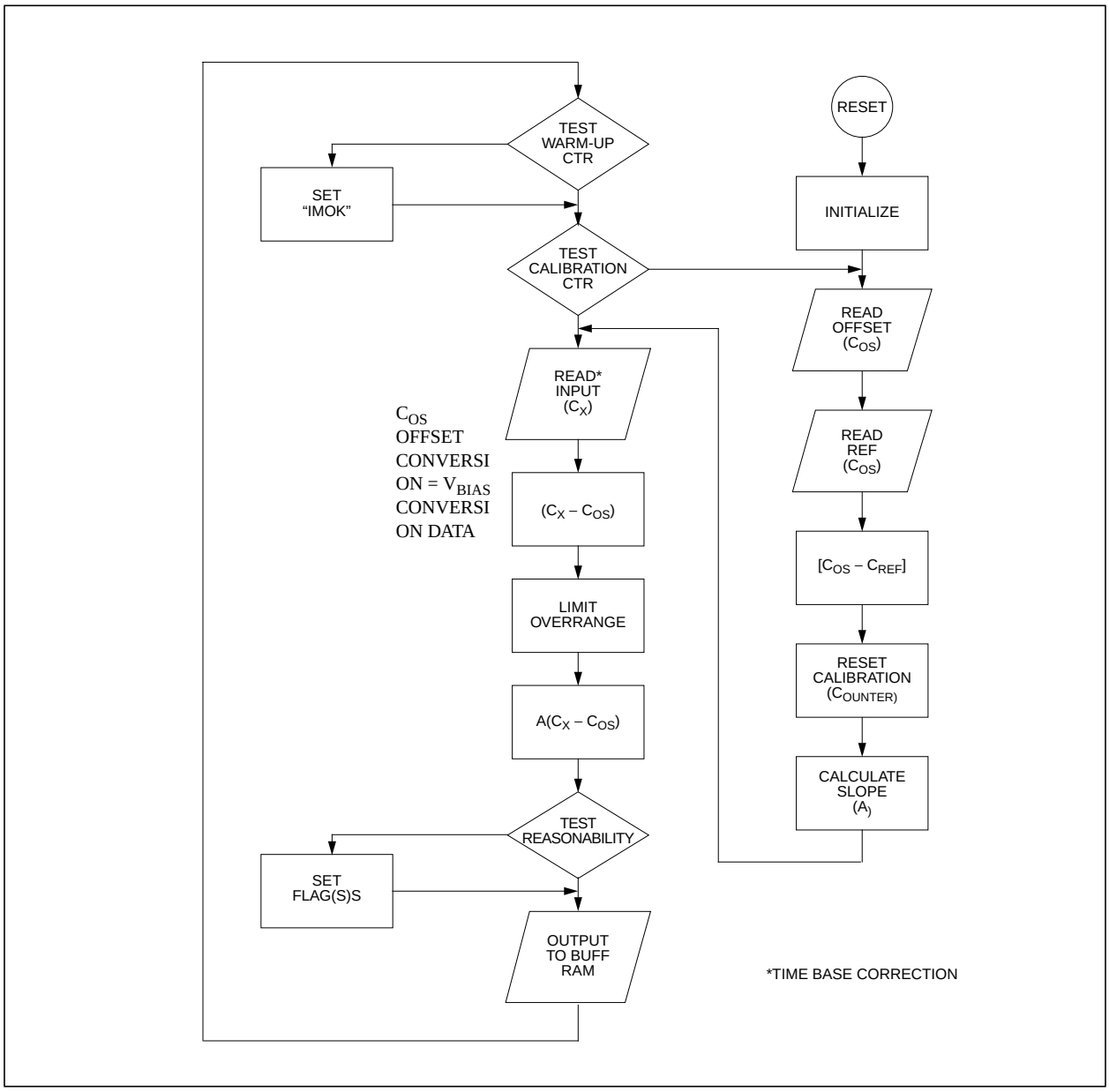

Figure 3-58. QAV Analog-to-Digital Conversion Process Flowchart

3-8.3. Specifications

Inputs

Point Sampling Rate (samples/second):

Note

QAV cards with prefixes of 5 or greater are selected for 50 or 60 Hz operation by jumper. The sampling rate is 4 per second and the sample period is 0.2 seconds for both 50 or 60 Hz operation.

- 4 at a power line frequency of 60 Hz
- 3.4 at a power line frequency of 50 Hz

Note

Once every 32 conversion, auto gain and auto zero calibration are performed; 8 seconds apart in 60 Hz systems, and 9.4 seconds apart in 50 Hz systems.

Resolution: 13-bits (includes polarity bit)

Input Channel Sample Period:

- 0.20 seconds at a power line frequency of 60 Hz
- 0.24 seconds at a power line frequency of 50 Hz

Normal Mode Voltage

- Surge: Meets IEEE/SWC test specifications without damage; however, the accuracy of data is reduced during, and up to 10 secs. after the removal of the surge.
- Continuous: An overrange of +120 VDC or 120 VAC rms at 50 or 60 Hz will not damage the input channels; however, a sustained overrange can affect subsequent data for several minutes following the removal of the overrange voltage.

Normal Mode Rejection

- 60 dB at 50 or 60 Hz using QTB card line frequency tracking or at 50 or 60 Hz +0.5 percent without QTB card
- 30 dB at 50 Hz +5 percent or 60 Hz +5 percent without QTB card line frequency tracking

Note

The input (peak-to-peak) AC voltage must not exceed 100 percent of the upper range value for specified accuracy and normal mode rejection.

Common Mode Voltage

- Surge: Meets IEEE/SWC test specifications without damage; however, the accuracy of data is reduced during, and up to 10 seconds following the removal of the surge.
- Continuous: A maximum of +500 VDC or peak AC can be applied without damage.

Common Mode Rejection

- 120 dB at DC and power line frequency and its harmonics with QTB card line frequency tracking or at 50 or 60 Hz +0.5 percent without QTB card
- 100 dB for nominal line frequency at +5 percent and harmonics without QTB card line frequency tracking

Note

Common mode rejection does not apply if the peak AC value exceeds 200,000 % of upper range value.

Input Impedance

- 10^7 Ω/Volt
- 10^3 Ω in overload

Reference Accuracy (per SAMA Standard PMC 20)

- +0.10 percent of the upper range value (+10 μV); +1/2 of the Least Significant Bit (LSB) at 99.7 percent confidence.
- Reference Conditions: 25°C + 1°C Ambient Temperature; 50 percent +2 percent of relative humidity; 0 V common mode; 0 V normal mode

Drift

- 0.002 percent per month (typical)
- 0.02 percent long term (typical)

Power Requirements

	Minimum	Nominal	Maximum
Primary Voltage:	12.4 VDC	+ 13.0 VDC	13.1 VDC
Optional Backup:	12.4 VDC	--	13.1 VDC
		Nominal	**Maximum**
Power Supply Current:		1.0 ADC	1.2 ADC
Power Used:		13.0 Watts	15.7 Watts

Input Signal Requirements

- G01 and G07 [1]cards: −5 to +20 mVDC, −20 to +20 mVDC at reduced accuracy[2]
- G02 and G08[1] cards: −12.5 to +50 mVDC, −50 to +50 mVDC at reduced accuracy[2]
- G03 and G09[1] cards: −25 to +100 mVDC, −100 to +100 mVDC at reduced accuracy[2]
- G04 cards: −12.5 to +50 mVDC, −50 to +50 mVDC at reduced accuracy[2]
- G05 cards: −25 to +100 mVDC, −100 to +100 mVDC at reduced accuracy[2]
- G06 cards: −12.5 to +50 mVDC, −50 to +50 mVDC at reduced accuracy[2]

Field signals are input to a standard Q series front-edge connector (see Figure 3-59). The DIOB address and DIOB address protection jumpers are also located in this connector. Each field signal input requires a plus, minus and shield pin.

[1]Level 8 QAV and later artwork support groups 1-3 **without** "On-Card" thermocouple compensation. Groups 7-9 are identical to Level 6 QAV groups 1-3 **with** "On-Card" thermocouple compensation. If "On-Card" thermocouple compensation is required, order groups 7-9 in place of groups 1-3 respectively

[2]Reduced reference accuracy is ±0.20 percent of the upper range value (±10 µV, ±1/2 LSB at 99.7 percent confidence.

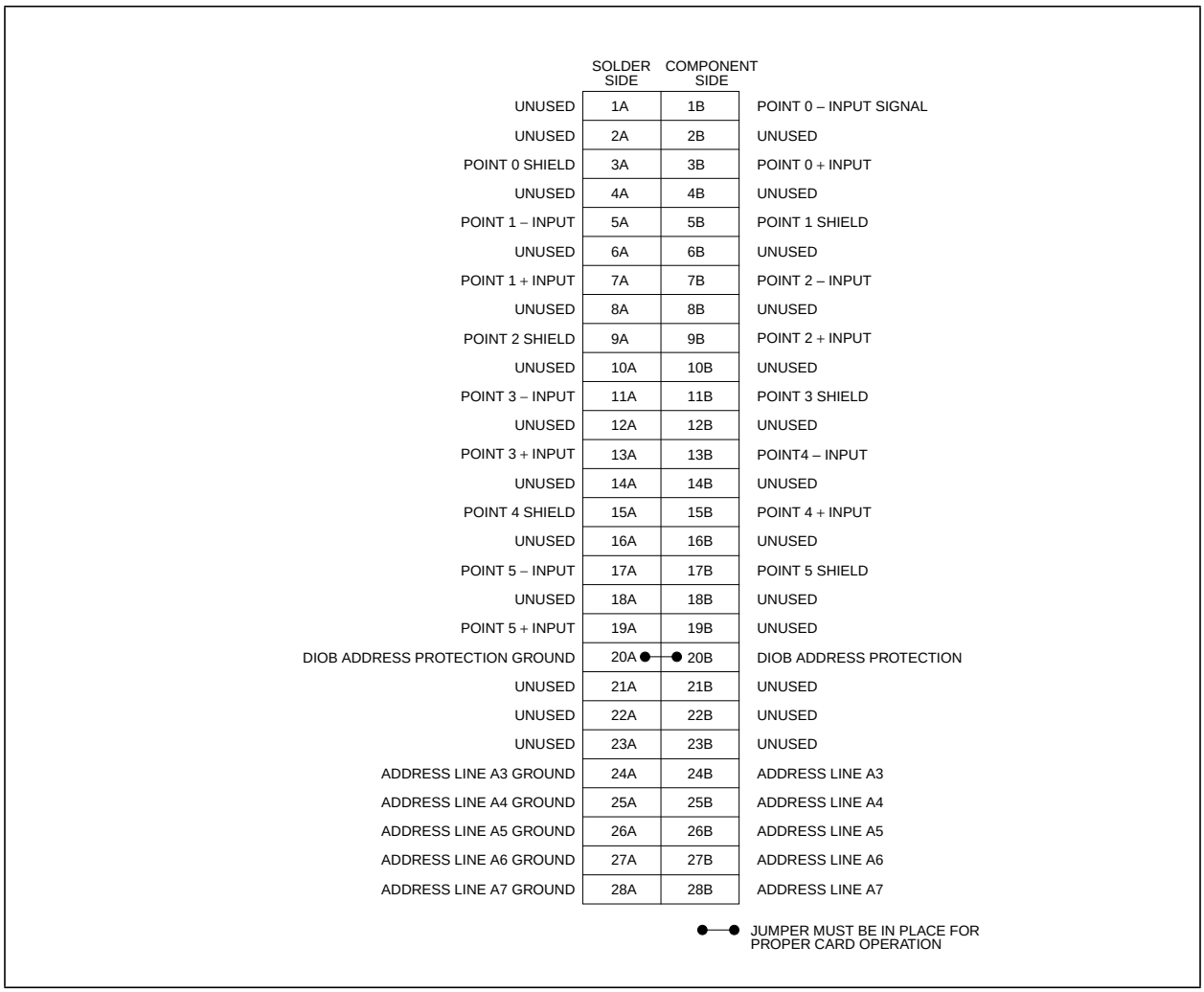

Figure 3-59. QAV Card Front-Edge Connector Pin Assignments

Output Signal Requirements

Output signal requirements are specified for DIOB requirements.

DIOB connection is made to the QAV card through the Q-card backplane connector to connector pins located on the rear-edge of the card (see Figure 3-60).

3-8.4. Card Addressing and Data Output

Address Jumpers

The QAV card address is established by five jumper fixtures which are located in the front-edge connector. The insertion of a jumper encodes a “1” on the selected address line (ADD3 through ADD7) which when matched by the DIOB address signals selects the QAV card by the system controller.

Figure 3-59 shows the pin configuration of the front-edge connector. The “B” pins of the connector are located on the component side and the “A” pins are located on the solder side of the card.

COMPONENT SIDE			SOLDER SIDE	
+V PRIMARY	2	1	+V PRIMARY	POWER
+V BACKUP	4	3	+V BACKUP	
GROUND	6	5	GROUND	
UADD1	8	7	UADD0	CARD ADDRESSING
UADD3	10	9	UADD2	
UADD5	12	11	UADD4	
UADD7	14	13	UADD6	
DATA-DIR	16	15	HI-LO	
DATA-GATE	18	17	UNIT*	CONTROL
DEV-BUSY	20	19	GROUND	
UDAT1	22	21	UDAT0	BIDIRECTIONAL DATA BUS
UDAT3	24	23	UDAT2	
UDAT5	26	25	UDAT4	
UDAT7	28	27	UDAT6	
$\overline{\text{UFLAG}}$*	30	29	GROUND	CONTROL
USYNC	32	31	$\overline{\text{UCAL}}$*	
GROUND	34	33	UCLOCK*	

* NOT USED ON QAV CARD

Figure 3-60. QAV Card Rear-Edge Connector Pin Assignments

QAV card addresses are programmed in groups of eight addresses in order to maintain the address recognition circuits at a minimum. However, cards equipped with the thermocouple temperature compensation feature use all eight addresses. Address 7 provides the temperature data, and address 8 is used during card calibration.

The addressing method allows up to 30 QAV cards to be used which means that 180 analog input channels can be provided (30 possibilities at a maximum of 6 channels per card yields 180 channels per DIOB controller).

Address protection is provided by a jumper insert on the front-edge connector pin pair (20A and 20B). This contact has been machined to be shorter than the other front-edge contacts so that it disconnects before the other contacts when the front card-edge connector is removed from the QAV card.

Output Data

Figure 3-61 shows a general, 16-bit, QAV card output data pattern format. The first 12 bits (0 through 11) are binary data obtained through a software routine in the QAV card microcomputer circuit.

The actual binary data that is sent to the system controller over the DIOB is calculated by the microcomputer using data from a precision voltage network and from an analog-to-digital converter circuit. Data from the precision voltage network is used to adjust the converted analog input (digital data) for offset and gain correction before it is output to the DIOB as point data.

Bit 12 is an overrange bit and bit 13 is a sign bit. A logic one signal at bit 12 indicates that the count data is in the positive overrange when bit 13 is at a logic zero and that the count data is in the negative range when bit 13 is a logical one. A logical zero at bit 12 indicates that the count data is in the negative overrange when bit 13 is a logical one and in the positive range when bit 13 is a logical zero. A logical one at bit 13 indicates the count is in the negative range and a logical zero at bit 13 indicates that the count is in the positive range.

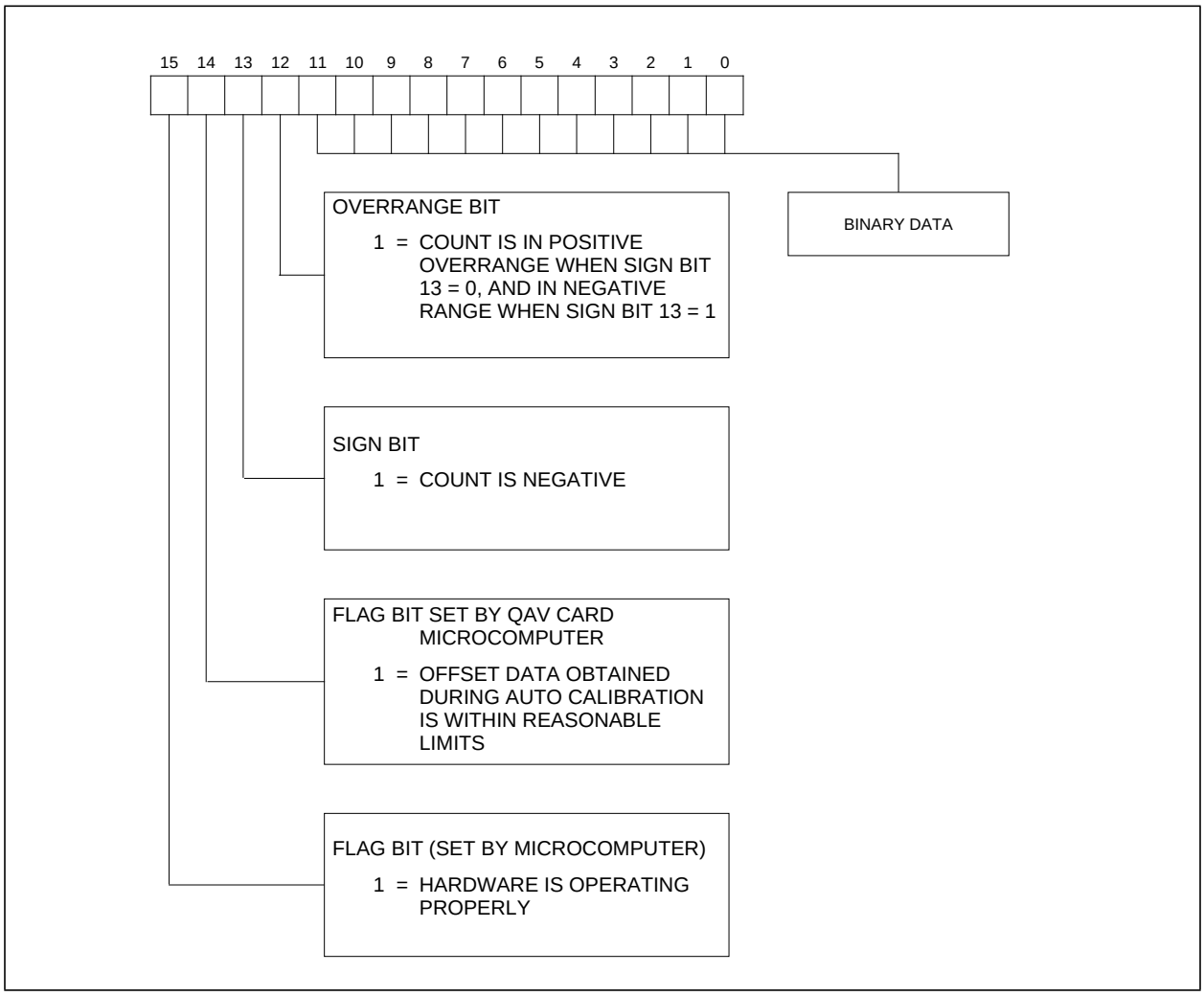

Figure 3-61. QAV Card Output Data Pattern Format

Bits 14 and 15 are flag bits. A logical one at bit 14 indicates that the offset factor data that was obtained during the auto-zero calibration microcomputer routine is within reasonable limits and a logical zero indicates unreasonable auto-zero data. A logical one at bit 15 (called IMOK bit) indicates that the hardware is operating properly (power is present, warm-up is complete, and the controller is operating). A logical zero at bit 15 indicates hardware trouble or that the offset factors from the auto-zero calibration are unreasonable on more than one input channel.

Note

Multiple channel offset errors will not set bit 15 on QAV cards with prefixes of 5 or greater.

Table 3-39 shows the nomenclature and the hexadecimal ranges for the QAV card output data. Note that bits 14 and 15 are set by QAV card microcomputer; therefore, the positive range to negative transitions occurs in 14 bits.

Table 3-39. QAV Card Output Data Ranges

Data Classification	Output Data Hexadecimal Code
Zero Input	C000
Positive Range	C001 to CFFF
Positive Full Scale	D000
Positive Overrange	D001 to DFFF
Negative Overrange	E001 to EFFF
Negative Full Scale	F000
Negative Range	F001 to FFFF
Out of Range Offset	8000 to BFFF
Card Hardware Trouble	0000 to 7FFF

3-8.5. Controls and Indicators (Level 6 and earlier)

The (Level 6 and earlier) QAV components are shown in Figure 3-62.

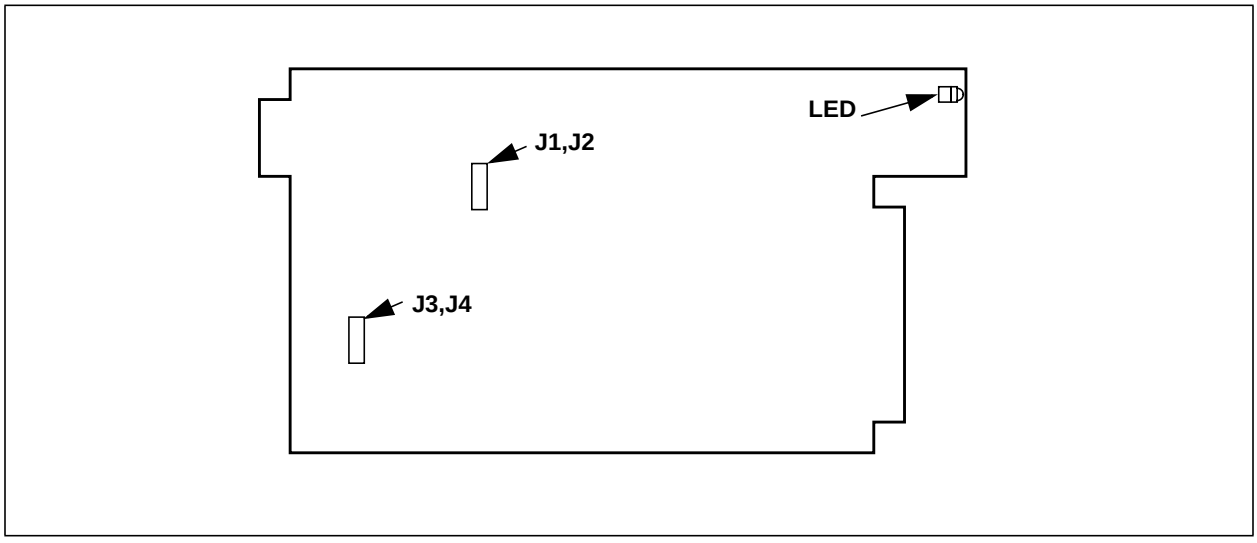

Figure 3-62. QAV Card Components (Level 6 and earlier)

Light Emitting Diodes (LED)

The QAV card has one LED which is used to indicate power “on”.